UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,331	07/20/2006	Henry Tan	2333-00900	9378

23505   7590   10/16/2008
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EXAMINER
SAVLA, ARPAN P

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
10/16/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pathou@conleyrose.com

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 July 2006</u>.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-14</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>1-14</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on <u>20 July 2006</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some *   c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>7/20/06, 1/14/08</u>.
4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/597,331 has a total of 14

claims pending, there are 2 independent claims and 10 dependent claims.

INFORMATION CONCERNING THE OATH/DECLARATION

Oath/Declaration

1.   Applicant's oath/declaration has been reviewed by Examiner and is found to

conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2.   Figures 1 and 2 should be designated by a legend such as --Prior Art-- because

only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3.　　　As required by MPEP § 609(c), Applicant's submission of the Information

Disclosure Statements dated July 20, 2006 and January 14, 2008 are acknowledged by

the Examiner and the cited references have been considered in the examination of the

claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449

initialed and dated by the Examiner is attached to the instant Office action.

OBJECTIONS

Specification

4.　　　The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

　　　　The following title is suggested: "A PORTABLE STORAGE DEVICE WHICH

SIMULTANEOUSLY WRITES TO MULTIPLE NAND FLASH MEMORY DEVICES"

5.　　　The abstract of the disclosure is objected to because the numerical references to

elements in the drawings should be removed from the abstract. Correction is required.

See MPEP § 608.01(b).

Claims

6.　　　**Claim 1** is objected to because the space between the word "buses" and the

comma and the space between the word "unit" and the comma, on lines 6 and 8

respectively, should be **deleted**.

7.   **Claim 1** is also objected to because the claim recites the limitation "the memory space" on line 20, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "memory space" (i.e. delete "the"). For the purposes of examining the instant application, the Examiner will interpret the limitation to read "memory space."

8.   **Claim 6** is objected to because the claim recites the limitation "the respective memory devices", however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "the respective NAND flash memory units." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "the respective NAND flash memory units."

9.   **Claim 8** is objected to because the claim recites the limitation "the respective **parallel** data buses", however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "the respective data buses." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "the respective data buses."

10.   **Claim 9** is objected to because the word "packets" on line 2 should instead read "packets."

11.   **Claim 13** is objected to because the claim recites the limitation "the memory space" on line 19, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "memory space" (i.e. delete "the"). For the purposes of examining the instant application, the Examiner will interpret the limitation to read "memory space."

12.   **Claims 2-12** are objected to because "A device according to claim…" should

instead read "The portable data storage device according to claim…"

13.   **Claim 14** is objected to because "**A** method of claim 13" should instead read

"**The** method of claim 13"

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

14.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

15.   **Claims 1-6, 8, 9, 13, and 14 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over Estakhri et al. (U.S. Patent 6,081,878) (hereinafter "Estakhri") in

view of Koh (U.S. Patent Application Publication 2003/0167376).

16.   **As per claim 1**, Estakhri discloses a portable data storage device including:

a data interface for transferring data into and out of the device (col. 6, lines 25-

27; Fig. 6b, element 610), *It should be noted that the "host interface" is analogous to*

the "data interface."

a master control unit (col. 6, lines 35; Fig. 6b, element 642); *It should be noted*

that the "flash state machine" is analogous to the "master control unit."

and at least two flash memory units connected to transfer data to and from the

master control unit via respective buses (col. 6, lines 45-49 and 54-64; Fig. 6a,

elements 670, 672, 675, 680, and 684); *It should be noted that the "first and second*
flash memory chips" are analogous to the "two flash memory units" and that "the first
and second buses (680 and 684)" are analogous to the "respective busses."

and the master control unit being arranged:

to partition data packets received from the interface into data packet portions
(col. 12, lines 11-17); *It should be noted that the "even and odd bytes" are analogous to*
the "data packet portions."

to transmit different ones of the data portions to each of the flash memory units
simultaneously using the respective data buses (col. 12, lines 11-17; Fig. 6a, elements
680 and 684);

and to control the flash memory units using control signals which are sent to both
the flash memory units (col. 11, lines 16-31; Fig. 9, elements 906, 908, 910, 912, and
914), the master control unit transmitting at least chip ENABLE signals to both the flash
memory units while transmitting the data portions using the buses (col. 11, lines 27-30;
col. 12, lines 11-17; Fig. 6a, elements 680 and 684; Fig. 9, element 914);

wherein the master control unit is further arranged to transmit a signal
simultaneously to the at least two flash memory units which causes the erasure of a
section of memory space of each of the at least two flash memory units (col. 19, lines
10-11 and 56-63; col. 20, lines 28-34; Fig. 14, element 906).

Estakhri does not disclose an interface controller;

the interface controller being arranged to send data received through the
interface to the master control unit;

and NAND flash memory units;

Koh discloses an interface controller (paragraph 0045; Fig. 5, element 120); *It should be noted that the "USB controller" is analogous to the "interface controller."*

the interface controller being arranged to send data received through the interface to the master control unit (paragraphs 0045-0047; Fig. 5);

and NAND flash memory units (paragraph 0046; Fig. 5, elements 22_1-22_n).

Estakhri and Koh are analogous art because they are from the same field of endeavor, that being flash memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Koh's USB connector/interface and USB controller within Estakhri's controller 510 as well as use Koh's NAND flash memory within Estakhri's flash memory chips because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of flash memory chips with higher densities and larger capacities at lower cost with faster erase, sequential write, and sequential read speeds by using NAND flash memory, as well as allowing the combined system to be compliant with the USB standard.

17.   **As per claim 2**, the combination of Estakhri/Koh discloses the NAND flash memory units are arranged to transmit simultaneously to the master control unit data packet portions, the master control unit being arranged to combine them to form data packets, and transmit the data packets to the interface controller for transmission

through the interface controller (Estakhri, col. 8, line 61 – col. 9, line 2; Koh, paragraphs 0045-0047).

18.   **As per claim 3**, the combination of Estakhri/Koh discloses there are two NAND flash memory units, and the master control unit is arranged to divide the data packets into data packet portions such that each word of the data to be stored is divided into two bytes which are included in data packet portions for different ones of the NAND flash memory units (Estakhri, col. 12, lines 11-29; Koh, paragraph 0046). *It should be noted that an "even byte" is stored in the "first flash memory chip" while an "odd byte" is stored in the "second flash memory chip."*

19.   **As per claim 4**, the combination of Estakhri/Koh discloses the master control units sends identical control signals simultaneously to both the NAND flash memory units through pins of the master control unit which are each electrically connected to a control signal line, each control signal line leading to respective control signal inputs of the each of the NAND flash memory units (Estakhri, col. 6, line 65 – col. 7, line 5; Fig. 6a, elements 690, 694, 696, 698, 702, and 704; Fig. 6b, elements 692 and 700; Koh, paragraph 0046).

20.   **As per claim 5**, the combination of Estakhri/Koh discloses the master control unit transmits identical WRITE, READ, ENABLE and ALE signals to the respective NAND flash memory units (Estakhri, col. 11, lines 20-31; Fig. 9, elements 908, 910, 912, and 914; Koh, paragraph 0046).

21.   **As per claim 6**, the combination of Estakhri/Koh discloses the interface is a USB interface, and the interface controller is a USB controller (Koh, paragraph 0045; Fig. 5, elements 21 and 121).

22.   **As per claim 8**, the combination of Estakhri/Koh discloses the respective data buses are 8-bit buses (Estakhri, col. 6, lines 59-64; Fig. 6a, elements 680 and 684).

23.   **As per claim 9**, the combination of Estakhri/Koh discloses each of the data packets has a predetermined size of 512 bytes (Estakhri, col. 7, lines 31-33).

24.   **As per claim 13**, Estakhri discloses a method of storing data in a portable data storage device including a data interface for transferring data into and out of the device, a master control unit having a cache memory, and at least two flash memory units, the method including the steps of:

      the master control unit partitioning the data packets received from the interface into data packet portions, and transmitting different ones of the data packet portions simultaneously to each of the flash memory units simultaneously through different respective buses (col. 6, lines 54-64; col. 12, lines 11-17; Fig. 6a, elements 675, 680, and 684), and controlling the flash memory units using control signals which are sent to both the flash memory units (col. 11, lines 16-31; Fig. 9, elements 906, 908, 910, 912, and 914), the master control unit transmitting WRITE instructions and chip ENABLE control signals to both the flash memory units (col. 11, lines 1-14, 27-30, and 48-52; Fig. 9, elements 902, 904, and 914), and subsequently, while still sending the chip ENABLE control signals, transmitting the data packet portions to the respective flash memory units using the respective buses (col. 12, lines 11-17; Fig. 6a, elements 680 and 684),

the respective flash memory units storing the data packet portions (col. 12, lines 17-29),

wherein the method further includes the step of the master control unit transmitting a signal simultaneously to the at least two flash memory units which causes the erasure of a section of memory space of each of the at least two flash memory units (col. 19, lines 10-11 and 56-63; col. 20, lines 28-34; Fig. 14, element 906).

Estakhri does not disclose an interface controller;

the interface controller being arranged to send data received through the interface to the master control unit;

and NAND flash memory units;

Koh discloses an interface controller (paragraph 0045; Fig. 5, element 120); *It should be noted that the "USB controller" is analogous to the "interface controller."*

the interface controller being arranged to send data received through the interface to the master control unit (paragraphs 0045-0047; Fig. 5);

and NAND flash memory units (paragraph 0046; Fig. 5, elements 22_1-22_n).

Estakhri and Koh are analogous art because they are from the same field of endeavor, that being flash memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Koh's USB connector/interface and USB controller within Estakhri's controller 510 as well as use Koh's NAND flash memory within Estakhri's flash memory chips because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods

with no change in their respective functions, and the combination would have yielded the predictable results of flash memory chips with higher densities and larger capacities at lower cost with faster erase, sequential write, and sequential read speeds by using NAND flash memory, as well as allowing the combined system to be compliant with the USB standard.

25.　　**As per claim 14**, the combination of Estakhri/Koh discloses retrieving data from a portable data storage device, the method including the steps of:

the master control unit issuing simultaneously to the flash memory units respective READ instructions and chip ENABLE signals (Estakhri, col. 8, lines 61-65);

the flash memory units in response to the READ instructions, and while still receiving the chip ENABLE control signals, transmitting simultaneously the data to the master control unit through different respective buses (Estakhri, col. 8, line 65 – col. 9, line 2);

the master control unit combining the data received from the flash memory units for form data packets and transmitting the data packets to the interface controller (Estakhri, col. 8, line 61 – col. 9, line 2; Koh, paragraphs 0045-0047);

and the interface controller sending data packets received from the master control unit out of the device through the data interface (Koh, paragraphs 0045-0047).

26.　　**Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of Koh as applied to claim 6 above, and further in view of EverythingUSB, "USB 2.0 FAQ - Information – Drivers" (hereinafter "USB 2.0").**

27. **As per claim 7**, the combination of Estakhri/Koh discloses all the limitations of claim 7 except the interface operates according to a USB standard in having a data transfer rate of at least 480 Mbits/s.

USB 2.0 discloses the interface operates according to a USB standard in having a data transfer rate of at least 480 Mbits/s (pg. 1, section titled "How fast is USB 2.0?").

The combination of Estakhri/Koh and USB 2.0 are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have obvious to a person of ordinary skill in the art to substitute USB 2.0's USB 2.0 specification for Estakhri/Koh's USB 1.1 specification because the simple substitution of one known element (USB 2.0 specification) for another (USB 1.1 specification) would have yielded the predictable results of a 40 times faster data rate which will in turn broaden the range of external peripherals that can be used on a computer as well as reduce bandwidth bottlenecks.

28. **Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of Koh as applied to claim 1 above, and further in view of Yamazaki et al. (U.S. Patent 5,699,297) (hereinafter "Yamazaki").**

29. **As per claim 10**, the combination of Estakhri/Koh discloses transmitting the signal to each of the NAND flash memory units which causes them to erase a section of their respective memory spaces (Estakhri, col. 19, lines 10-11 and 56-63; col. 20, lines 28-34; Fig. 14, element 906; Koh, paragraph 0046).

The combination of Estakhri/Koh does not disclose the master control unit is operative to instruct each NAND flash memory unit to transfer a portion of the data stored in that section of the memory space to a different location.

Yamazaki discloses the master control unit is operative to instruct each NAND flash memory unit to transfer a portion of the data stored in that section of the memory space to a different location (col. 3, lines 30-34 and 46-55; Fig. 1, elements 1, 2, and 9). *It should be noted that the "erase and write control circuit" is analogous to the "master control unit" and the "RAM" is analogous to the "different location."*

The combination of Estakhri/Koh and Yamazaki are analogous art because they are from the same field of endeavor, that being flash memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to couple Yamazaki's temporary evacuation RAM to Estakhri/Koh's NAND flash memory chips because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of preventing retained data (i.e. unmodified data) from being degraded due to the driving of the flash memory during an erase operation.

30.   **As per claim 10**, the combination of Estakhri/Koh/Yamazaki discloses the different location is in a RAM memory (Yamazaki, col. 3, lines 46-55; Fig. 1, element 2).

31.   **Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of Koh as applied to claim 1 above, further in view of Yamazaki et**

as applied to claim 10 above, and even further in view of Hasbun et al. (U.S.

Patent 5,581,723).

32.   **As per claim 12**, the combination of Estakhri/Koh/Yamazaki discloses all the

limitations of claim 12 except the different location is in a location in the respective

memory spaces outside the section which is to be erased.

Husbun discloses the different location is in a location in the respective memory

spaces outside the section which is to be erased (col. 9, lines 44-58; col. 10, lines 14-

17; Fig. 4, elements 57 and 61).

The combination of Estakhri/Koh/Yamazaki and Hasbun are analogous art

because they are from the same field of endeavor, that being flash memory systems.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to implement Hasbun's cleanup/erase procedure to

Estakhri/Koh/Yamazaki's flash memory chips because all the claimed elements were

known in the prior art and one skilled in the art could have combined the elements as

claimed by known methods with no change in their respective functions, and the

combination would have yielded the predictable results of providing a means for reliably

storing block structure data during an erase operation in a flash memory array.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the

application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-14** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1.   U.S. Patent 5,822,245 (Gupta et al.) discloses a flash memory array architecture comprising a flash memory array, first and second memory buffer, and I/O interface circuit which has several operating modes which permit data to be read from the flash memory array, several operating modes which permit data to be programmed into the flash memory array, and a mode for rewriting the data in the flash memory array.

2.   U.S. Patent 5,890,192 (Lee et al.) discloses concurrent write of multiple chunks of data into multiple subarrays of flash EEPROM.

3.   U.S. Patent 6,426,893 (Conley et al.) discloses a flash EEPROM system with simultaneous multiple data sector programming and storage of physical block characteristics in other designated blocks.

4.   U.S. Patent 6,571,312 (Sugai et al.) discloses a data storage method and data processing device using an erasure block buffer and write buffer for writing and erasing data in memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
September 24, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185